Micro-Research Finland Oy
Välitalontie 83 C, FI-00660 Helsinki, Finland

Event Receiver (PMC-EVR)

Technical Reference

Contents

Introduction

Event Receivers (EVR) recover the clock signal from the event stream transmitted by an Event Generator and generate an event clock that is phase locked to the Event Generator event clock and thus to the RF reference. Event Receivers convert event codes transmitted by an Event Generator to hardware outputs. They can also generate software interrupts and store the event codes with globally distributed timestamps into FIFO memory to be read by a CPU module from the VME bus.

Functional Description

After recovering the event clock the Event Receiver demultiplexes the event stream to the 8-bit distributed bus and the 8-bit event code. The Event Receiver provides two mapping RAMs. While one of the RAMs is active, the other one may be modified from VME. The event code is applied to the address lines of the active mapping RAM. The 16-bit data programmed into a specific memory location pointed to by the event code determines what actions will be taken. In addition to the mapping RAMs each of bit 0 to 6 of the event code may generate a trigger event which is a pulse with the length of a single event cycle. There are also a few special event codes to reset prescaler outputs, control the timestamp event counter and reset the heartbeat timeout counter.

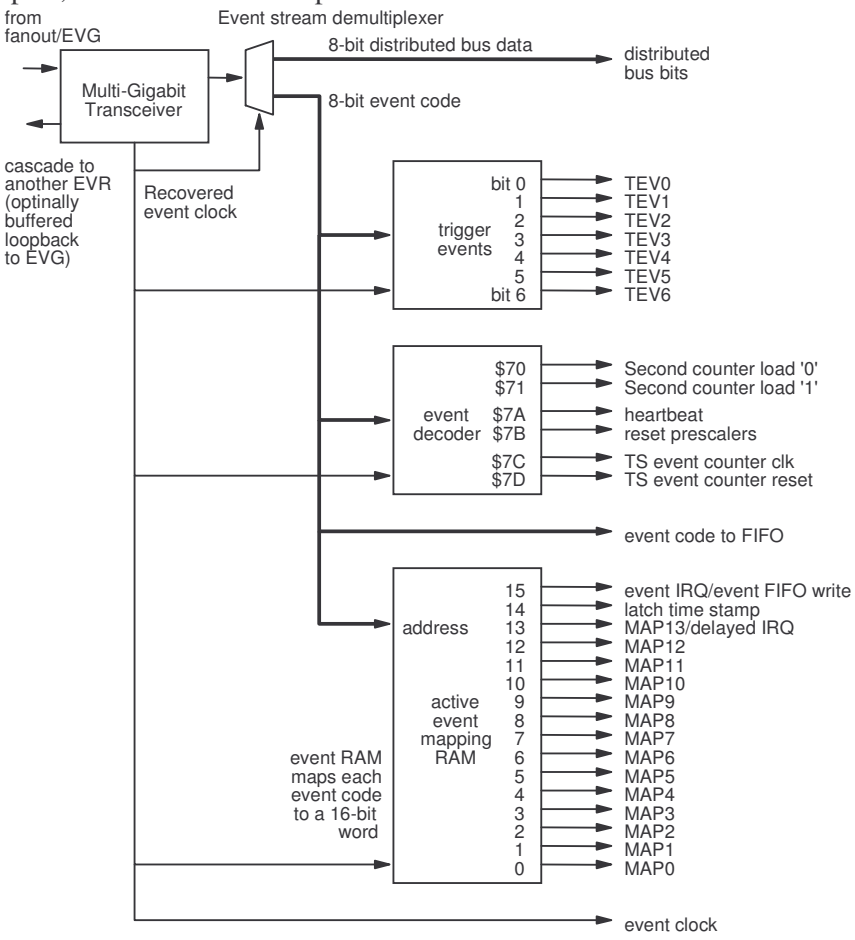

Figure 1: Event Stream Decoding

A heartbeat monitor is provided to receive heartbeat events (event code $7A). The heartbeat counter is reset upon receiving the heartbeat event code. If no heartbeat is received the counter times out (approx. 1.6 s) and a heartbeat flag is set. The Event Receiver may be programmed to generate a heartbeat interrupt.

Timestamp Events

The Event System provides a global timebase to attach timestamps to collected data and performed actions. The time stamping system consists of a 32-bit timestamp event counter and a 32-bit seconds counter. The timestamp event counter either counts received timestamp counter clock events or runs freely with a clock derived from the event clock. The timestamp event counter is cleared upon receiving a timestamp event counter reset event. The seconds counter is updated serially by loading zeros (event code $70) and ones (event code $71) into a shift register MSB first. The seconds register is updated from the shift register when the timestamp event counter is cleared.

The timestamp event counter and seconds counter contents may be latched into a timestamp latch. Latching is determined by the active event map RAM and may be enabled for any event code.

An event FIFO memory is implemented to store selected event codes with attached timing information. The 80-bit wide FIFO can hold up to 511 events. The recorded event is stored along with 32-bit seconds counter contents and 32-bit timestamp event counter contents at the time of reception. The event FIFO as well as the timestamp counter and latch are accessible from VME.

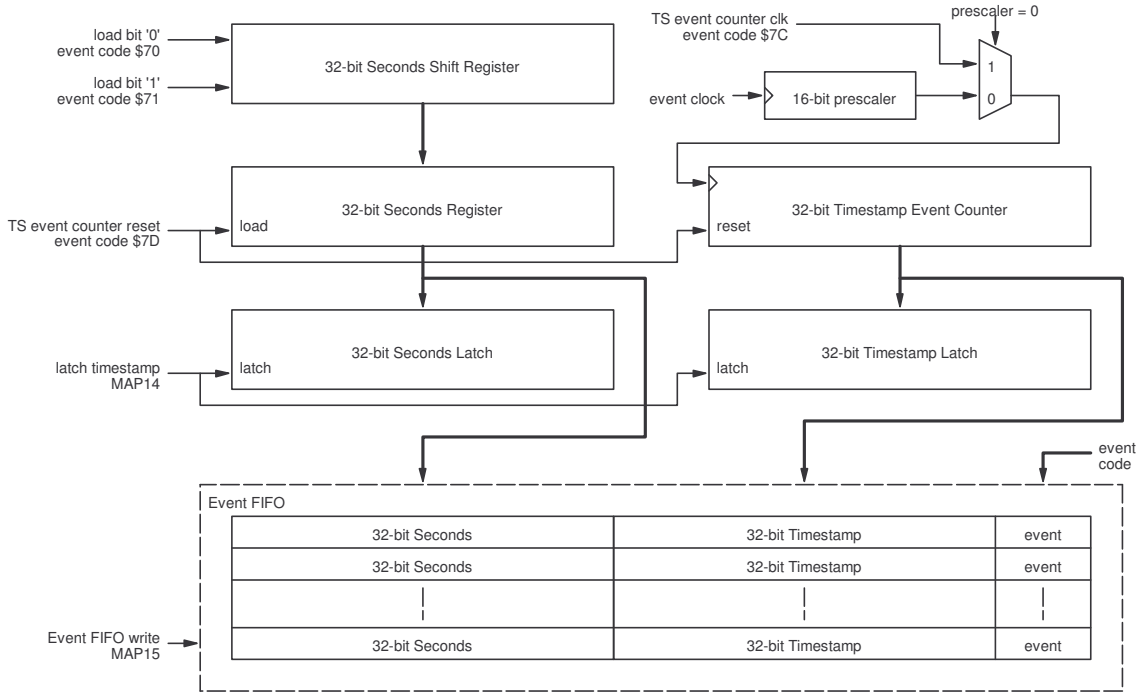

Figure 2: Event FIFO and Timestamping

Hardware Outputs

The Event Receiver can generate up to 32 simultaneous outputs on the VME P2 connector. Transition modules provide TTL and optical outputs. The outputs may be selected from multiple sources. There are also a few outputs available in the front panel.

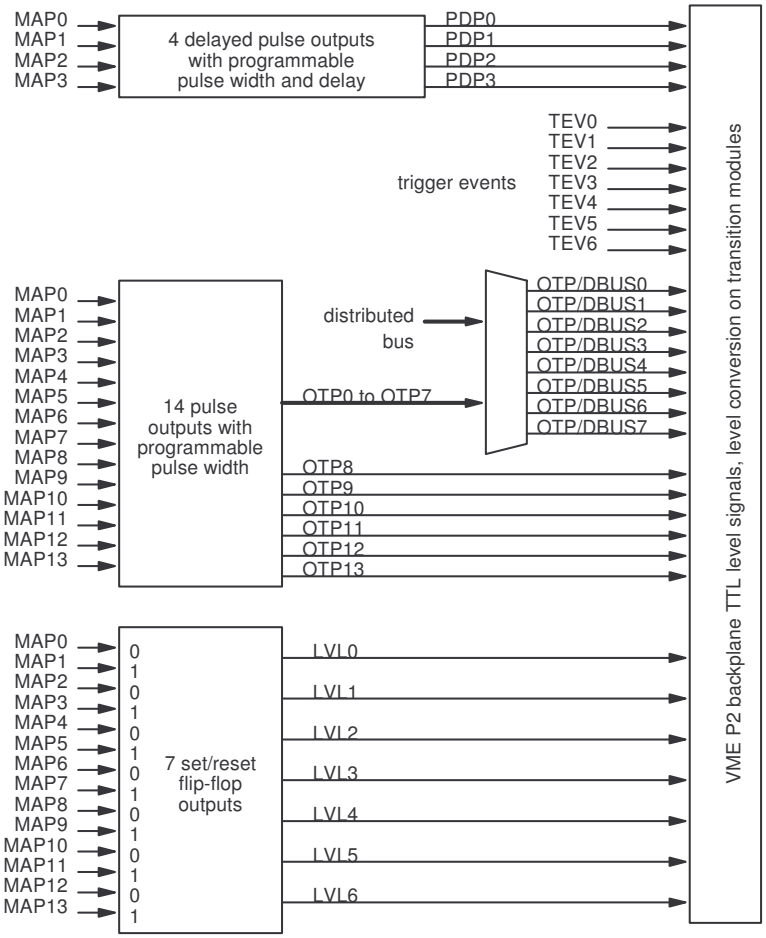

Figure 3: Event Receiver Hardware Outputs

There are fourteen pulse outputs (called OTP for historical reasons) of programmable delay, width and polarity. For each channel the pulse delay may be adjusted from 0 to 32^2-1 event clock cycles (up to 34.3 s with event clock of 125 MHz) and the pulse width may be adjusted from 1 to 65535 event clock cycles (8 ns to 524 µs with event clock of 125 MHz). Eight pulse outputs share the output pin with the distributed bus signals. The mapping (pulse/distributed bus pin) for each of the shared pins may be selected independently.

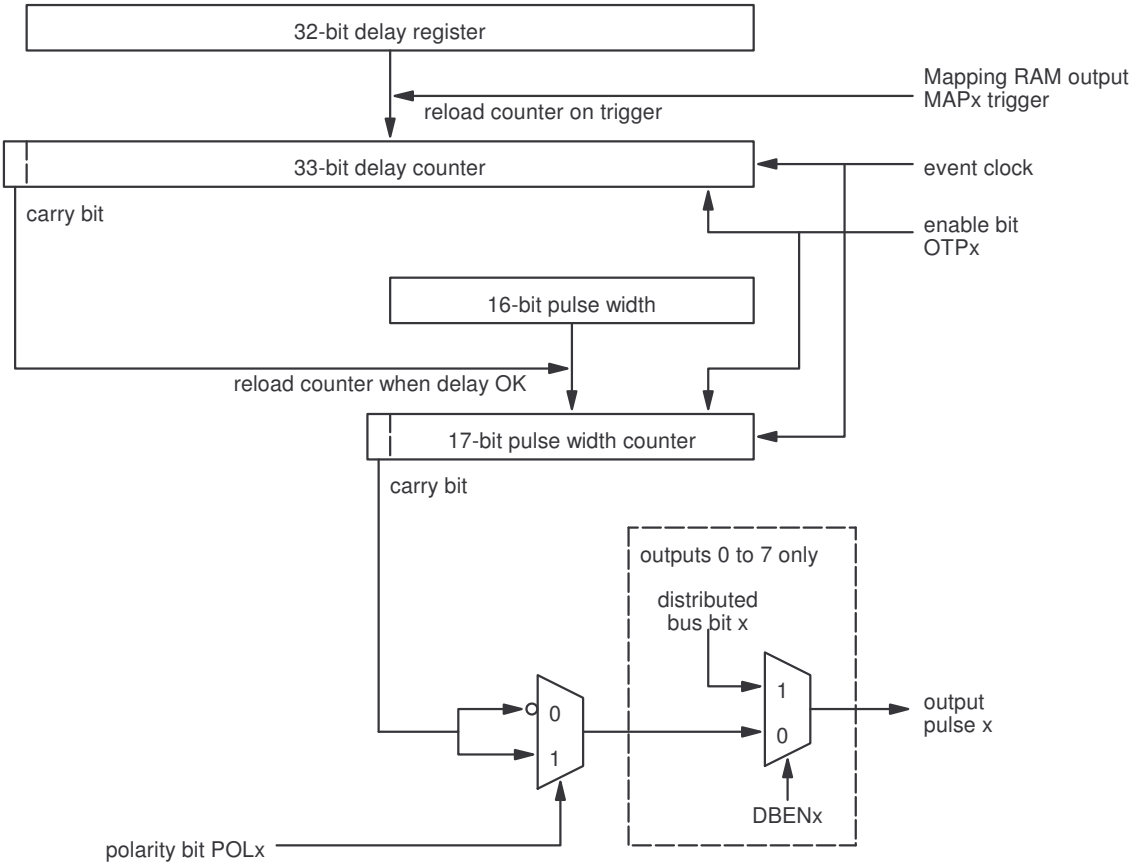

Figure 4: Programmable Width Pulse Outputs

Flip flop outputs may be programmed to change their state on desired event codes.

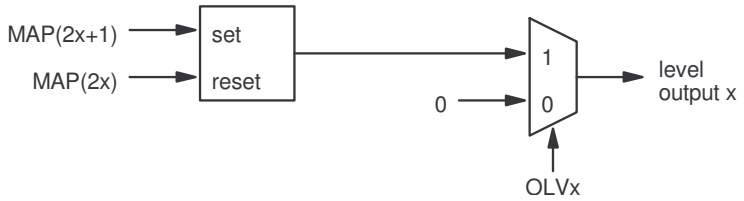

Figure 5: Level Outputs

Four extended delayed pulse outputs (called DGP for historical reasons) provide programmable delay, width and polarity like the pulse outputs. The delay and width counters share a 16-bit programmable prescaler which generates counting frequencies from event clock/65536 to the event clock rate. The delay and width counters both are 32-bits wide and thus allow maximum delays and pulse widths up to 625 h at event clock rate of 125 MHz.

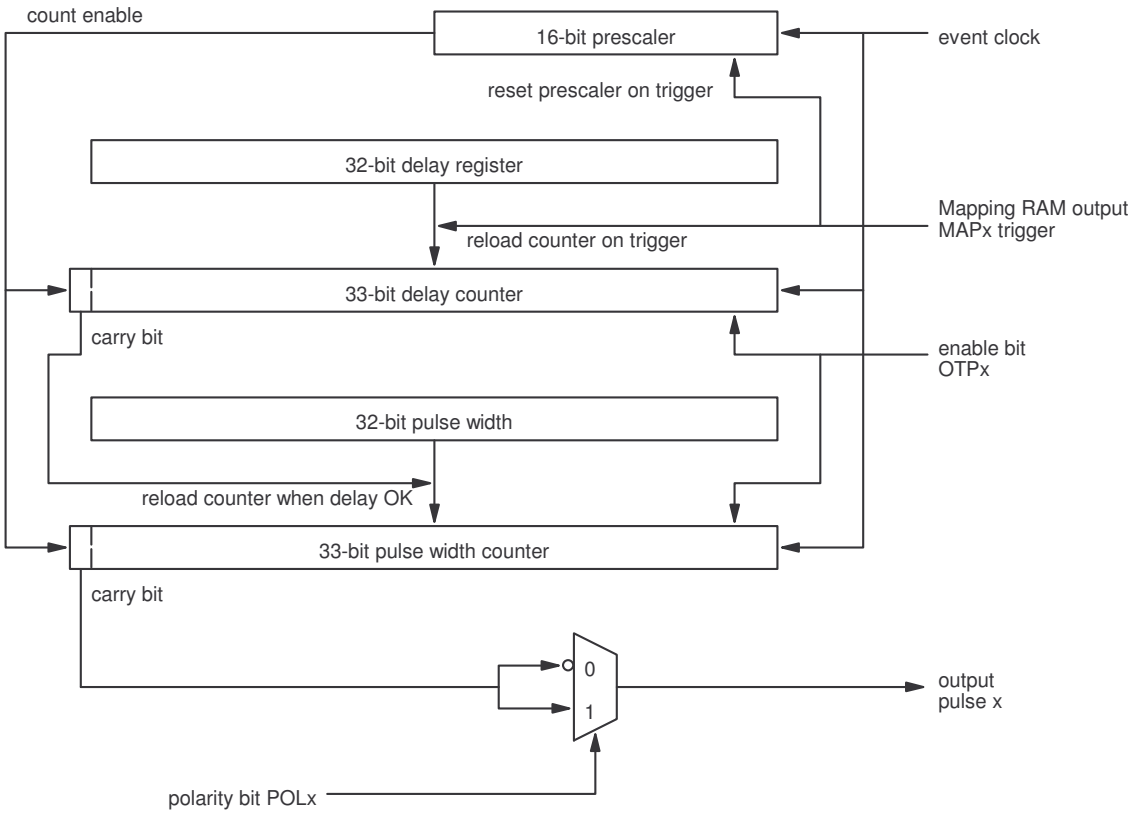

Figure 6: Programmable Delayed Pulse Outputs

Bits 0 to 6 of the received event code may be used to generate trigger event outputs. The width of a trigger event is one event clock cycle.

Prescaler Outputs

The Event Receiver provides three programmable prescaler outputs which may be mapped to front panel outputs. The frequencies are divided from the event clock. A special event code reset prescalers $7B causes the prescalers to be synchronously reset, so the frequency outputs will be in same phase across all event receivers.

Interrupt Generation

The Event Receiver has multiple interrupt sources which all have their own enable and flag bits. The following events may be programmed to generate an interrupt:

- Receiver violation: bit error or the loss of signal.
- Lost heartbeat: heartbeat monitor timeout.
- Write operation of an event to the event FIFO.
- Event FIFO is full.

In addition to the events listed above a delayed interrupt is provided. The delayed interrupt is triggered by event map RAM bit 13. A 16-bit prescaler running with the event clock frequency and a 16-bit delay counter determine the interrupt delay.

External Event Input

An external hardware input is provided to be able to take an external pulse to generate an internal event. This event will be handled as any other received event.

Programmable Reference Clock

The event receiver requires a reference clock to be able to synchronise on the incoming event stream sent by the event generator. For flexibility a programmable reference clock is provided to allow the use of the equipment in various applications with varying frequency requirements.

Fractional Synthesiser

The clock reference for the event receiver is generated on-board the event receiver using a fractional synthesiser. A Micrel (http://www.micrel.com) SY87739L Protocol Transparent Fractional-N Synthesiser with a reference clock of 24 MHz is used. The following table lists programming bit patterns for a few frequencies.

Event Rate	Configuration Bit Pattern	Reference Output	Precision (theoretical)
499.654 MHz/4 = 124.9135 MHz	0x0C928166	124.907 MHz	-52 ppm
50 MHz	0x009743AD	50.0 MHz	0

The event receiver reference clock is required to be in ±100 ppm range of the event generator event clock.

Connections

Front Panel Connections

The front panel of the PMC Event Receiver is shown in Figure 7.

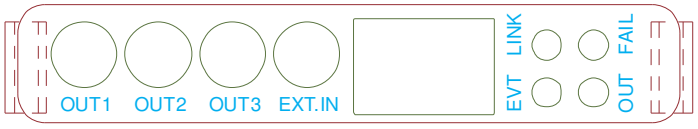

Figure 7: Event Receiver Front Panel

The front panel of the Event Receiver includes the following connections and status leds:

Connector / Led	Style	Level	Description
LINK	Green Led		Receiver Link Signal OK
EVT	Yellow Led		Incoming Event (RX)
OUT	Yellow Led		Active HW output
FAIL	Red Led		Receiver Violation
TX (SFP) next to leds	LC	Optical 850 nm	Event link Transmit
RX (SFP) next to EXT.IN	LC	Optical 850 nm	Event link Receiver
OUT1	LEMO-EPL	TTL	Programmable TTL Output 1
OUT2	LEMO-EPL	TTL	Programmable TTL Output 2

OUT3	LEMO-EPL	TTL	Programmable TTL Output 3
EXT IN	LEMO-EPL	TTL	External Event Input

PMC Pn4 User I/O Pin Configuration

The following table lists the connections to the PMC Pn4 User I/O Pins and to VME P2 pins when the module is mounted on a host with "P4V2-64ac" mapping complying VITA-35 PMC-P4 to VME-P2-Rows-A,C.

PMC Pn4 pin	VME P2 Pin	Signal
2	A1	Transition board ID0
4	A2	Transition board ID1
6, 8, …, 20	A3-A10	Ground
22	A11	Transition board ID2
24	A12	Transition board ID3
26, 28, 30	A13-A15	Ground
32	A16	Transition board handle switch
34, 36, …, 52	A17-A26	Ground
54, 56, …, 62	A27-A31	+5V
64	A32	Power control for transition board
1	C1	delayed pulse output 0
3	C2	delayed pulse output 1
5	C3	delayed pulse output 2
7	C4	delayed pulse output 3
9	C5	trigger event output 0
11	C6	trigger event output 1
13	C7	trigger event output 2
15	C8	trigger event output 3
17	C9	trigger event output 4
19	C10	trigger event output 5
21	C11	trigger event output 6
23	C12	programmable width pulse / distributed bus output 0
25	C13	programmable width pulse / distributed bus output 1
27	C14	programmable width pulse / distributed bus output 2
29	C15	programmable width pulse / distributed bus output 3
31	C16	programmable width pulse / distributed bus output 4
33	C17	programmable width pulse / distributed bus output 5
35	C18	programmable width pulse / distributed bus output 6
37	C19	programmable width pulse / distributed bus output 7
39	C20	programmable width pulse output 8
41	C21	programmable width pulse output 9
43	C22	programmable width pulse output 10
45	C23	programmable width pulse output 11

47	C24	programmable width pulse output 12
49	C25	programmable width pulse output 13
51	C26	level output 0
53	C27	level output 1
55	C28	level output 2
57	C29	level output 3
59	C30	level output 4
61	C31	level output 5
63	C32	level output 6

Programming Details

Register Map

Address Offset	Register	Type	Description
0x000	Control	UINT16	Control/Status Register
0x002	MapAddr	UINT16	Mapping RAM Address Register (8 bit)
0x004	MapData	UINT16	Mapping RAM Data Register
0x006	PulseEnable	UINT16	Output Pulse Enable Register
0x008	LevelEnable	UNIT16	Level Output Enable Register
0x00A	TriggerEnable	UINT16	Trigger Pulse Enable Register
0x00C	EventCounter	UNIT32	Timestamp Event Counter
0x010	TSLatch	UINT32	Timestamp Latch
0x014	EventFIFO	UINT32	Event FIFO bits 31 - 8 – 24 LSB of Timestamp Counter bits 7 - 0 – Event Code
0x018	PDPEnable	UINT16	Delayed Pulse Enable Register
0x01A	PDPSelect	UINT16	Delayed Pulse Select Register
0x01C	PDPDelay	UINT16	Series 100 Compatible Multiplexed Delay Register (16 LSB only)
0x01E	PDPWidth	UINT16	Series 100 Compatible Multiplexed Width Register (16 LSB only)
0x020	(reserved)	UINT16	(reserved)
0x022	IrqEnable	UINT16	Interrupt Enable Register
0x024	DBusEnable	UINT16	Distributed Bus Enable Register
0x026	DBusData	UINT16	Distributed Bus Data Register
0x028	PDPPrescaler	UINT16	Multiplexed Prescaler Register
0x02A	EventPrescaler	UINT16	Event Counter Prescaler Register
0x02C	(Reserved)	UINT16	(Reserved)
0x02E	FirmwareVersion	UINT16	Event Receiver Firmware Version

			Register
0x040	FPMap1	UINT16	Front Panel TTL Output 1 Map Register
0x042	FPMap2	UINT16	Front Panel TTL Output 2 Map Register
0x044	FPMap3	UINT16	Front Panel TTL Output 3 Map Register
0x046	(reserved)	UINT16	(reserved)
0x048	(reserved)	UINT16	(reserved)
0x04A	(reserved)	UINT16	(reserved)
0x04C	(reserved)	UINT16	(reserved)
0x04E	UsecDivider	UINT16	Divider to get from Event Clock to 1 MHz
0x050	ExtEvent	UINT16	External Event Code Register
0x052	(reserved)	UINT16	(reserved)
0x054	SecondsSR	UINT32	Seconds Shift Register
0x058	TSSec	UINT32	Timestamp Latch Seconds Register
0x05C	(Reserved)	UINT32	(Reserved)
0x060	EvFIFOSec	UINT32	Event FIFO Seconds Register
0x064	EvFIFOEvCnt	UINT32	Event FIFO Event Counter Register
0x068	OutputPolarity	UINT32	Output Polarity Register (for pulse outputs)
0x06C	ExtDelay	UINT32	Multiplexed Delay Register
0x070	ExtWidth	UINT32	Multiplexed Width Register
0x074	Prescaler_0	UINT16	Prescaler 0 divider
0x076	Prescaler_1	UINT16	Prescaler 1 divider
0x078	Prescaler_2	UINT16	Prescaler 2 divider
0x07A	TrBoardIO	UINT16	Transition Board IO
0x07C	(Reserved)	UINT32	(Reserved)
0x080	FracDiv	UINT32	SY87739L Fractional Divider Configuration Word

Control and Status Register

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x000	EVREN	IRQEN	RSTS	HRTBT	IRQFL	LTS	MAPEN	MAPRS

Bit	Function
EVREN	Event Receiver Master enable.
IRQEN	VME irq enable. When 0 all interrupts are disabled.
RSTS	Write 1 to reset timestamp event counter and timestamp latch.
HRTBT	Lost heartbeat flag. Write 1 to reset.
IRQFL	Event FIFO interrupt flag. Write 1 to reset.
LTS	Write 1 to latch timestamp from timestamp event counter to timestamp latch.
MAPEN	Event mapping RAM enable.
MAPRS	Mapping RAM select bit for event decoding. 0 - mapping RAM 1, 1 - mapping RAM 2.

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x001	LDFS	VMERS		DIRQ	RSFIFO	FF	FNE RSDIRQ	RXVIO

Bit	Function
LDFS	Writing a '1' to this bit location forces a reload of the Micrel fractional synthesizer configuration word
VMERS	Mapping RAM select bit for VME access. 0 - mapping RAM 1, 1 - mapping RAM 2.
DIRQ	Delayed interrupt flag.
RSFIFO	Write 1 to clear event FIFO.
FF	Event FIFO full flag. Write 1 to reset flag.
FNE	FIFO not empty flag. Indicated whether there are event in event FIFO.

Mapping RAM address register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x003	Mapping RAM common address register							

Mapping RAM data register

address	bit 15	bit 0
0x004	Mapping RAM common data register	

Output pulse enable register

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x006			OTP13	OTP12	OTP11	OTP10	OTP9	OTP8

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x007	OTP7	OTP6	OTP5	OTP4	OTP3	OTP2	OTP1	OTP0

Bit	Function
OTPx	Enable programmable width output pulse x.

Output level enable register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x009		OLV6	OLV5	OLV4	OLV3	OLV2	OLV1	OLV0

Bit	Function
OLVx	Enable level output pulse x.

Trigger event enable register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x00B		TEV6	TEV5	TEV4	TEV3	TEV2	TEV1	TEV0

Bit	Function
TEVx	Enable trigger event output pulse x.

Timestamp event counter register

address	bit 15															bit 0
0x00C	Timestamp event counter (LSW, read only)															

address	bit 15															bit 0
0x00E	Timestamp event counter (MSW, read only)															

Timestamp event latch register

address	bit 15															bit 0
0x010	Timestamp event latch (LSW, read only)															

address	bit 15															bit 0
0x012	Timestamp event latch (MSW, read only)															

Event FIFO data register

address	bit 15								bit 8
0x014	Event FIFO data register, bits 7 – 0 of timestamp event counter								

address	bit 7								bit 0
0x015	Event FIFO data register, event code								

address	bit 15															bit 0
0x016	Event FIFO data register, bits 23 – 8 of timestamp event counter															

Programmable delayed pulse output enable register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x019	POL3	POL2	POL1	POL0	PDP3	PDP2	PDP1	PDP0

Bit	Function
POLx	Delayed pulse output x polarity: 0 - active high, 1 - active low.
PDPx	Delayed pulse output x enable.

Programmable pulse / delay select register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x01b				DSEL4	DSEL3	DSEL2	DSEL1	DSEL0

DSEL	Register selected
00000	Programmable delayed pulse 0
00001	Programmable delayed pulse 1
00010	Programmable delayed pulse 2
00011	Programmable delayed pulse 3
00100	Delayed interrupt
10000	Programmable width pulse 0
10001	Programmable width pulse 1
10010	Programmable width pulse 2
10011	Programmable width pulse 3

10100	Programmable width pulse 4
10101	Programmable width pulse 5
10110	Programmable width pulse 6
10111	Programmable width pulse 7
11000	Programmable width pulse 8
11001	Programmable width pulse 9
11010	Programmable width pulse 10
11011	Programmable width pulse 11
11100	Programmable width pulse 12
11101	Programmable width pulse 13

Programmable Delayed Pulse / Delayed Interrupt Delay Register

address	bit 15	bit 0
0x01C	Programmable Delayed Pulse / Delayed Interrupt Delay Register	

Programmable Width Pulse / Delayed Pulse Width Register

address	bit 15	bit 0
0x01E	Programmable Width Pulse / Delayed Pulse Width Register	

Interrupt configuration register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x023				IEDIRQ	IEEVT	IEHRT	IEFF	IEVIO

Bit	Function
IEDIRQ	Delayed interrupt enable.
IEEVT	Event interrupt enable.
IEHRT	Lost heartbeat interrupt enable.
IEFF	Event FIFO full interrupt enable.
IEVIO	Receiver violation interrupt enable.

Distributed bus enable register

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x025	DBEN7	DBEN6	DBEN5	DBEN4	DBEN3	DBEN2	DBEN1	DBEN0

Bit	Function
DBENx	OTPx output select: 0 - programmable width pulse x, 1 - distributed bus bit x.

Distributed bus data register

address	bit 7	bit 0
0x027	Distributed bus data register (read only)	

Programmable Delayed Pulse / Delayed Interrupt Prescaler Register

address	bit 15	bit 0
0x028	Programmable Delayed Pulse / Delayed Interrupt Prescaler Register	

Timestamp Event Counter Clock Prescaler Register

address	bit 15	bit 0
0x02A	Timestamp Event Counter Clock Prescaler Register	

Front Panel Output Multiplexer Registers

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x040			FP1SEL5	FP1SEL4	FP1SEL3	FP1SEL2	FP1SEL1	FP1SEL0
0x042			FP2SEL5	FP2SEL4	FP2SEL3	FP2SEL2	FP2SEL1	FP2SEL0
0x044			FP3SEL5	FP3SEL4	FP3SEL3	FP3SEL2	FP3SEL1	FP3SEL0

FPxSEL *)	Signal selected
000000	Programmable Delayed Pulse Output 0
000001	Programmable Delayed Pulse Output 1
000010	Programmable Delayed Pulse Output 2
000011	Programmable Delayed Pulse Output 3
000100	Trigger Event Output 0
000101	Trigger Event Output 1
000110	Trigger Event Output 2
000111	Trigger Event Output 3
001000	Trigger Event Output 4
001001	Trigger Event Output 5
001010	Trigger Event Output 6
001011	Programmable Width Pulse Output 0
001100	Programmable Width Pulse Output 1
001101	Programmable Width Pulse Output 2
001110	Programmable Width Pulse Output 3
001111	Programmable Width Pulse Output 4
010000	Programmable Width Pulse Output 5
010001	Programmable Width Pulse Output 6
010010	Programmable Width Pulse Output 7
010011	Programmable Width Pulse Output 8
010100	Programmable Width Pulse Output 9
010101	Programmable Width Pulse Output 10
010110	Programmable Width Pulse Output 11
010111	Programmable Width Pulse Output 12
011000	Programmable Width Pulse Output 13
011001	Level Output 0
011010	Level Output 1
011011	Level Output 2
011100	Level Output 3
011101	Level Output 4
011110	Level Output 5
011111	Level Output 6
100000	Distributed Bus Data 0
100001	Distributed Bus Data 1
100010	Distributed Bus Data 2
100011	Distributed Bus Data 3
100100	Distributed Bus Data 4

100101	Distributed Bus Data 5
100110	Distributed Bus Data 6
100111	Distributed Bus Data 7
101000	Prescaler 0
101001	Prescaler 1
101010	Prescaler 2

*) FP1 to FP3 are front panel TTL outputs 1 to 3

External Event Code Register

address	bit 7	bit 0
0x051	External Event Code Register	

Seconds Shift Register

address	bit 31	bit 0
0x054	Seconds Shift Register (read-only)	

Timestamp Latch Seconds Register

address	bit 31	bit 0
0x058	Timestamp Latch Seconds Register (read-only)	

Event FIFO Extended Timestamp Registers

address	bit 31	bit 0
0x060	Event FIFO Seconds Register (read-only)	
0x064	Event FIFO Event Counter Register (read-only)	

Polarity Register

address	bit 31	bit 30	bit 29	bit 28	bit 27	bit 26	bit 25	bit 24
0x068								POL24

address	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0x069	POL23	POL22	POL21	POL20	POL19	POL18	POL17	POL16

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
0x06A	POL15	POL14	POL13	POL12	POL11			

address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x068					POL3	POL2	POL1	POL0

Bit	Function
POL0-3	Programmable Delayed Pulse Output Polarity 0 – normal polarity (pulse active high) 1 – inverted polarity
POL11	Output Pulse 0 (OTP0) Polarity 0 – normal polarity (pulse active high) 1 – inverted polarity
…	…

POL24 Output Pulse 13 (OTP13) Polarity
0 – normal polarity (pulse active high)
1 – inverted polarity

SY87739L Fractional Divider Configuration Word

address	bit 31	bit 0
0x080	SY87739L Fractional Divider Configuration Word	

Configuration Word	Frequency with 24 MHz reference oscillator
0x0C928166	124.907 MHz
0x018741AD	119 MHz
0x009743AD	50 MHz
0xC25B43AD	49.978 MHz

Note: to reload the configuration word to the fractional synthesizer a ‘1’ has to be written to the control register LDFS bit (see description of control register starting on page 10). Changes will not take effect until the configuration word is reloaded.